TECH TIME Helpful Tips for the Avionics Technician

BY AL INGLE

This month, we continue our series on serial busses. Having previously discussed their evolution, we now focus on how this information is distributed throughout an aircraft without data corruption.

There are a number of limitations on how fast data can be transferred:

1. The transmitter has an upper limit on how fast it can reliably process and send a data stream.
2. The receiver has an upper limit on how fast it can reliably receive and process a data stream.
3. The signaling medium (copper wires/fiber/wireless) has an upper limit on how fast it can carry a data stream.
4. Industry standards and the need for compatability with other equipment.

There are two ways to express data transmission rates: ***baud*** and ***bits per second*** (***bps***). ***Baud*** describes the signaling rate of individual bits that *could* be carried by a databus. It is specifically defined as the reciprocal of the shortest element or bit in the system, in seconds. For example, if you have a buss with a 10 µS element or bit, the baud is 1 bit/10 x 10^{-6} seconds or 100K bits per second. Note that because baud is by definition a rate per second, you do not speak of a baud rate, only baud. The signaling rate in baud does not tell you the actual information rate of that buss – only its upper limit for a continuous stream. The maximum information transfer is defined as the number of equivalent binary digits transferred per second; this is measured in ***bits per second*** (***bps***). One packet of *bits* is typically called a ***byte*** or ***word***.

Our industry utilizes the simplest binary data encoding, whereby each signaling element equals one bit. More sophisticated encoding schemes can deliver more information, one of which is the quadrature-phase-shift keying (QPSK) scheme. It utilizes a 90° phase transition to represent a level shift, thereby increasing the information capacity of a single bit by two. Why is this and other exotic types of encoding not used in aircraft? Because they are complicated and susceptible to corruption in harsh electrical/RF environments.

Within a given piece of equipment, or system of components, it is desirable to use the highest possible data rate. Because data transfers are subject to errors, there should be some additional method of detecting, and where possible, correcting errors. The ***parity*** bit is the most common type of error detection. This bit is added to the bit stream and selected such that the number of high or "1" bits (data bits plus parity bit) is either even or odd, as defined by the protocol. The receiver (slave) adds up the number of high bits and if correct, the data is assumed to be correct. Note that a randomly chosen word has a 50 percent chance of even or odd parity; therefore, at first glance, the parity bit appears to provide minimal assurance of integrity. However, on relatively error-free data busses, the predominant error is of the one bit type, which maximizes the parity bit's protection.

There are two distinct types of serial busses in our industry: ***synchronous*** and ***asynchronous.***

The ***synchronous*** buss derives its bit timing integrity through 1) the use of a second conductor carrying the clock signal to keep the bits in sync; and 2) a third conductor to gate the duration of the byte and/or to reset both the shift register in the transmitter (master) and the receiver (slave).

This three-wire scheme is found throughout our society in many variations. In the consumer sector, we have Microwire (National Semiconductor), SPI (Motorola), and I^2C (Philips). In our industry, we are most familiar with Bendix/King's three-wire synchronous buss in use since the late 1970s. This buss has been tailored to the requirements of the data to be sent; for example, its DME channeling buss has a different bit structure than its RNAV databus because of the wide variation in information to be sent. The enable gate can vary from a single start pulse to a length spanning the duration of the transmission. The bit number varies from a low of 10 to a high of 64 (*See Figure 1).*

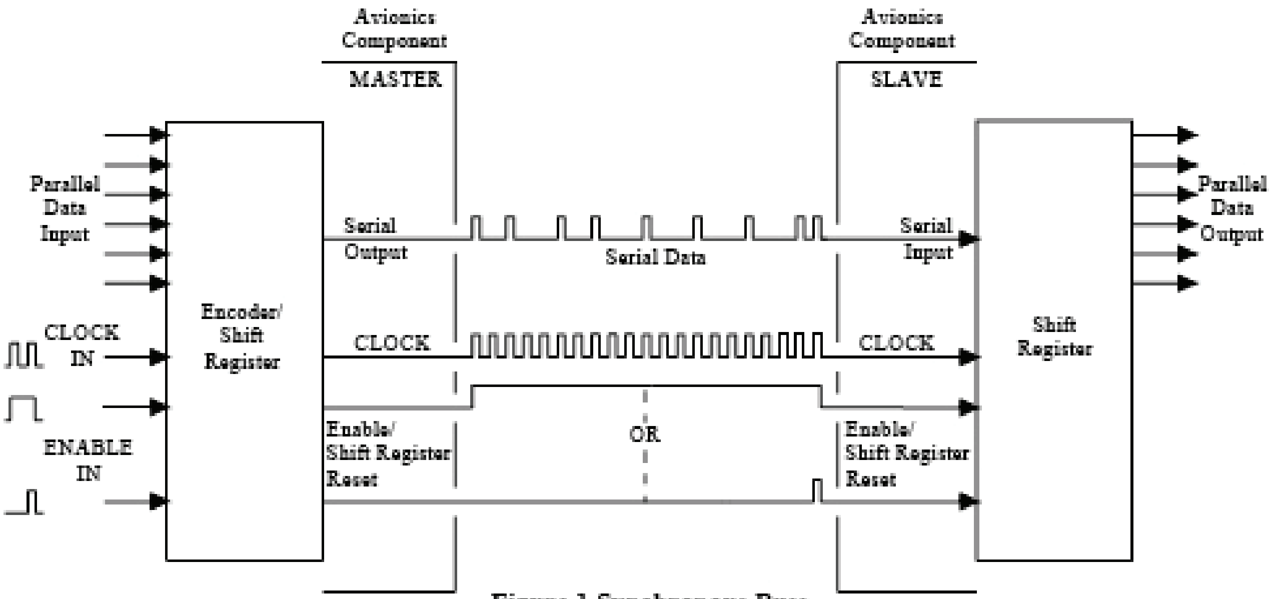

Figure 1 Synchronous Buss

The ***asynchronous*** buss derives its bit timing integrity through the use of a ***start*** and ***stop*** bit and near universal use of the parity bit and/or other error-detection schemes. The receiver waits for the initial bit to reset its shift register and counts from that point in time. Asynchronous busses can have as few as a single conductor (and common return), but typically operate as differential pairs for maximum immunity from noise and common-mode (ground) induced errors.

RS-232 is an example of a single conductor buss (with common ground) utilized extensively in our office environment with a short effective range. RS-232, operated as a differential pair, extends its useful range considerably and becomes RS-422. Rockwell Collins' CSDB serial buss is similar to RS-422. ARINC 429, ubiquitous in our industry, operates as a differential pair and adds the tri-state buss to further minimize corruption of data and maximize error detection *(See Figure 2)*.

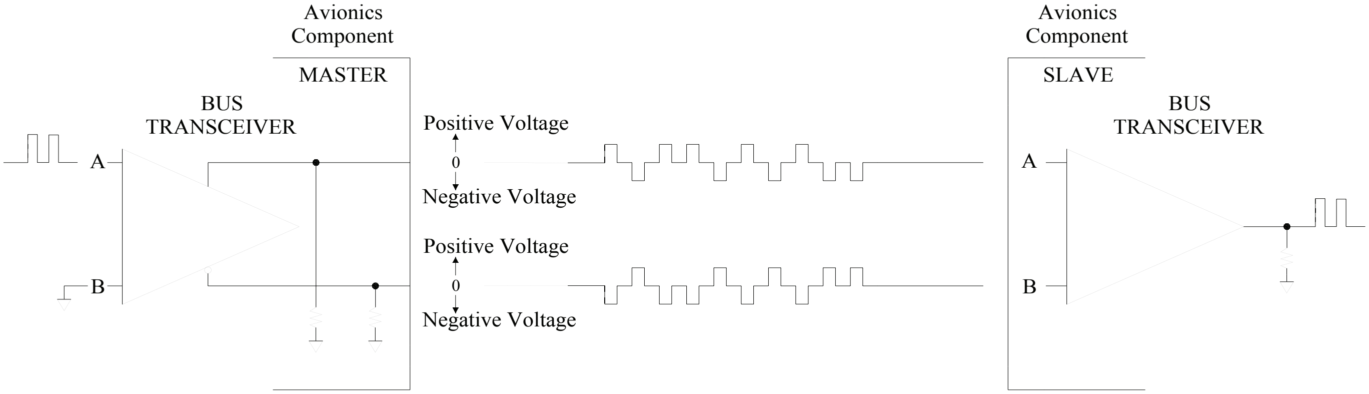

Figure 2 Asynchronous Buss

With today's state-of-the-art technology and manufacturing processes, line replaceable units are robust and reliable transmitters and receivers of serial data. The weak link in the information exchange is the aircraft wiring and its environment.

References: "Coding SPI Software," *EDN*, Dec. 3, 2007, pages 55-60, www.edn.com
"Communications: Internal and External Interfacing," The 2007 *ARRL Handbook for Radio Communications*, pages 5.67-5.70

Next Month: More Serial Busses